An Integrated 2GHz 500mW Bipolar Amplifier

Dr. S. Weber, G. Donig

Siemens AG Dept. HL HF E, Munich, Germany

A low cost integrated 2GHz 500mW amplifier for DECT and other applications is presented. The total efficiency is 35% with a 3.3V supply voltage and 5dBm input signal. The chip is based on the Siemens B6HF 26GHz-f_T-technology and is to our knowledge the first commercial 500mW 2GHz amplifier in bipolar technology. The device also features functions which are previously not available from PA IC´s including power down, power selection and supply voltage compensation.

The chip contains a full balanced two-stage RF amplifier and the complete biasing/power ramping circuit. Also a power select function for power saving reasons is included via logic pin PSEL. The low power mode (P_{out}≤23dBm) may be used if the handy is near the base station. In the power down mode (controlled via logic pin PAON) the supply current is typically less than 1µA, therefore the expensive supply voltage switch (typically a MOSFET or a pnp transistor with some passive components), which is normally needed in GaAs designs, is not required. Figure 1 shows the totally different layout of our design compared to more conventional GaAs PAs.

Figure 2 shows the simplified schematic. The first RF stage is an emitter-coupled differential pair. Via an internal LC-matching network the output of the first stage is connected to the base inputs of the common emitter push-pull output stage. The Q-Faktor of the on-chip inductor elements is about 6 to 7 which is sufficient for this purposes. Q is limited due to substrate losses (ρ_{Si}=8Ωcm) and the metallization (about 15mΩ per square for 2 Al layers). The overall linear gain is 30dB. The output power in both high and low power mode is set by external resistors and the internal bandgap reference to control the bias current of the first RF stage. The class of operation and therefore linearity and efficiency is set by further resistors which controls the output stage bias current. Linearity is not a main problem in DECT systems due to the simple GFSK modulation scheme. All bias currents are optimized to get a constant RF output power even in the presence of temperature or V_{CC} changes (look at $R_{VCCK/L}$ of figure 3). The nominal supply voltage range is 3V to 4.5V. The amplifier features high stability, easy bypassing and low distortion (especially even harmonics) due to the balanced architecture. Further advantages are the higher impedance levels (for easier and more efficient matching networks) and the possibility to use a standard small outline package. The differential output signal may be converted to a ground referred 50Ω signal via a lumped printed balun (see figure 3). It acts like a high pass filter from output pin PO to the 50Ω port and as a low pass from the inverted pin POX. Both pathes together build a wide band allpass circuit with the needed 180° phase shift between PO and POX at DECT center frequency. The symmetrical 50Ω input of the amplifier is designed to interface with our DECT-RX/TX-IC´s PMB4420 and 4220 with no extra stage, but even an unbalanced input operation is possible. Another way to build a RX/TX system is to use a symmetrical antenna (loop or dipole antenna) for the TX path and perhaps a conventional ground referred antenna for the LNA. One advantage of this configuration is the possibility to ommit all RF switches (different polarization of the antennas) and to minimize filtering (very low distortions in the PA due to symmetry, higher TX efficiency and lower RX noise figure). This may compensates the costs for the second antenna.

Extensive simulations with the SABER (Analogy) time domain simulator and the APLAC harmonic balance simulator (University of Helsinki) has been made in the design process. These simulations and some test designs are showing a better performance (efficiency and stability) for the LC coupled amplifier in respect to some DC coupled amplifier designs. In all RF simulations it is very important to include all on and off chip parasitic elements and to use transistor models, which are accurate in the whole bias range. It also appears that it is not possible to design the linear transformation networks only by linear simulation. Therefore we use the harmonic balance simulator APLAC on a PC to optimize the balun elements

in conjunction with the nonlinear output stage. For the design of on-chip spiral inductors an interactive PC-program is under development. Even first investigations are showing the wide area of coil design to be conquered : simple spiral coils, coils with one or more taps, symmetrical coils, lateral and vertical coupled coils and many others topologies have to be optimized for different applications like filters and oscillators and different frequency ranges and layout restrictions. For this reason many test inductors (E6 series and special structures like transformers) and field simulations have been made.

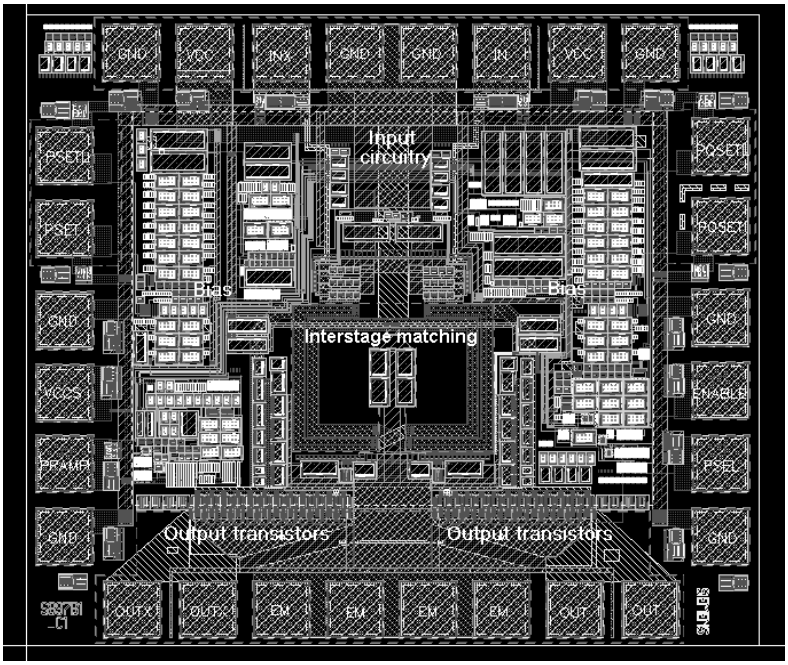
The device is to our knowledge the first commercial integrated bipolar DECT amplifier. The main advantages in respect to the discrete and GaAs-MMIC competitors are : no supply switch needed, no negative supply voltage required, lower costs and intelligent features like power select and supply voltage compensation. Also new is the fully balanced architecture which is especially advantageous for the integration of precise and complex building blocks due to low substrate noise level and high common mode rejection. The PA is delivered in a small sized enhanced P-TSSOP-28 (outer dimensions 10mm x 6mm) package with 10 ground pins. In this package the amplifier works with duty cycles up to 50% which is important for fast hopping (uses all DECT time slots) base station applications. For handies and slow hopping base stations a smaller package is possible. A 2.4GHz PA for ISM applications is also available. This device has smaller output transistors and a slightly modified interstage matching network with smaller inductors and capacitors.

Currently amplifiers for PCN (1800MHz and 2W) and GSM (900MHz and 4W) are under development. These designs should contain the complete power adjusting circuitry. Dependend on the input power level a two-stage (P_{in} = +5..+15dBm for up-conversion loop systems) and a three-stage amplifier (P_{in} = 0dBm for conventional systems) is implemented.

Technical parameters of the DECT-PA

- symmetrical bipolar 500mW PA
- η = 35% at V_{CC}=3,3V
- power down and ramping included
- power select function
- V_{CC}- and temperature compensation
- designed to operate with PMB4420/4220
- P-TSSOP 28 package

Figure 1 : Layout of the PA



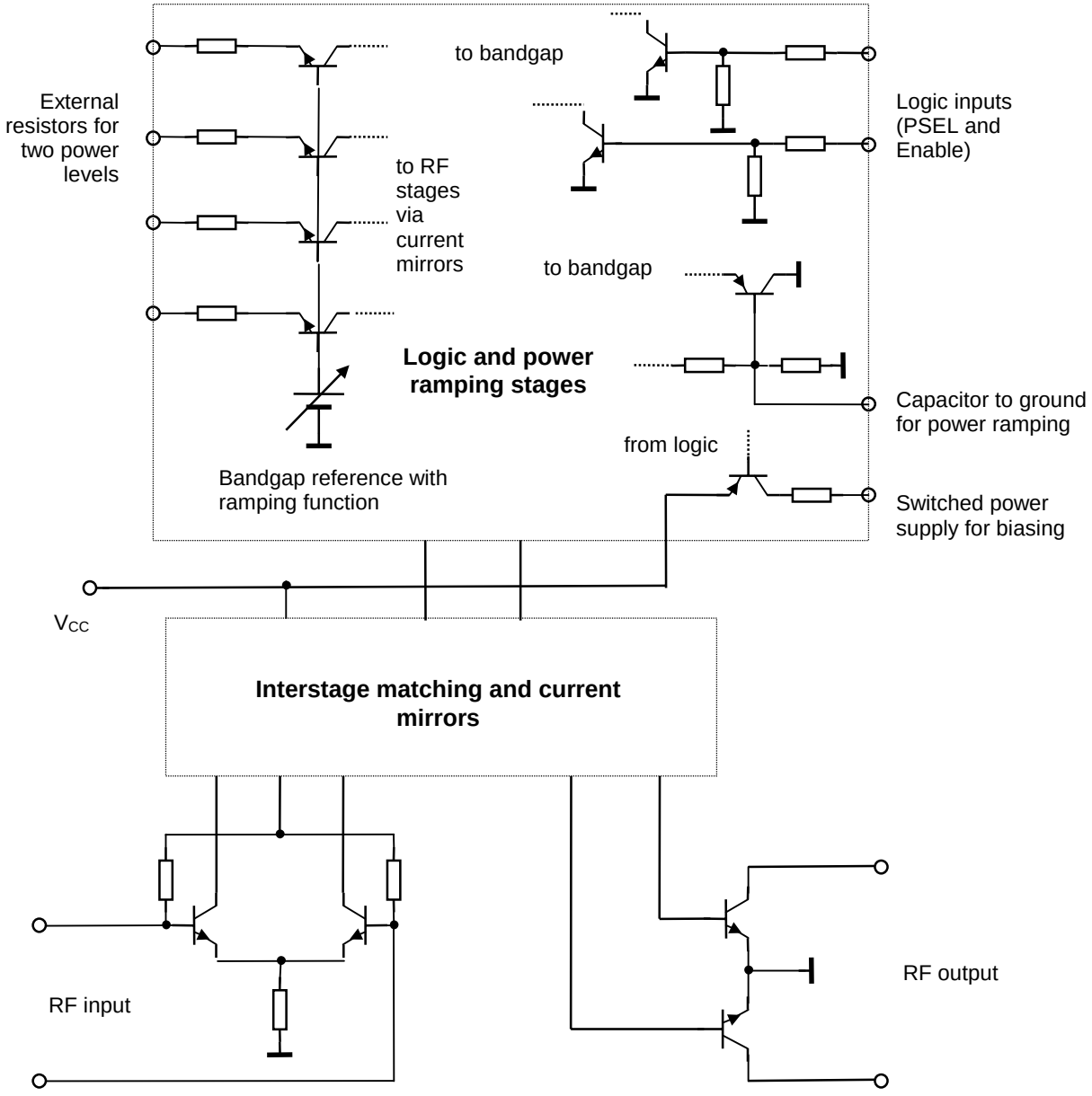


Figure 2 : Simplified schematic

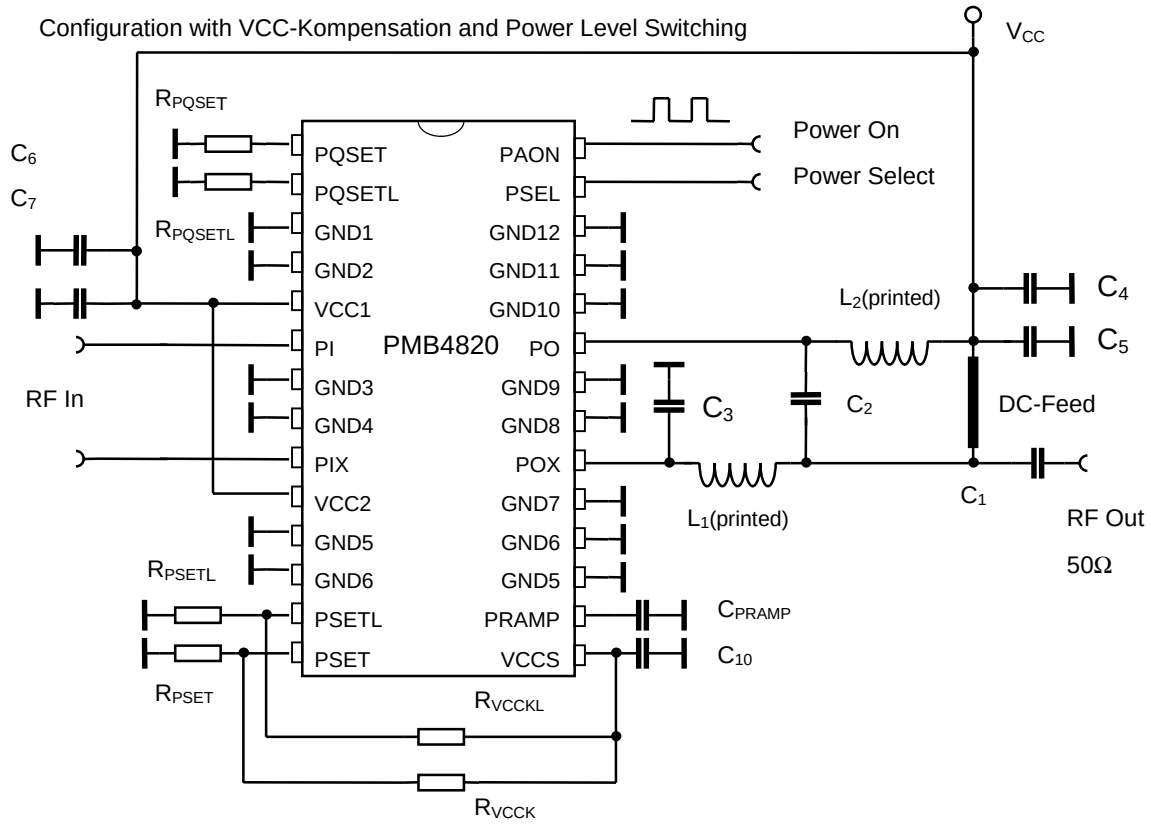


Figure 3 : Application with balanced input for interface with PMB4420 DECT receiver