Power Controller for Dual Band TDMA Power Amplifiers

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Abstract **An Si IC for the analog power control of a TDMA dual-band power amplifier featuring a low-pass filter, internal RF detectors and a loop amplifier is presented. The key design constraints are identified and an optimized system topology with a new gain-shaping block is developped.**

I. Introduction

TDMA systems have been covered the whole world, e.g. the GSM900/1800/1900 cellular phone network. One key task is the design of a circuitry for accurate control of transmit power versus time. But this is often overlooked and still many manufacturers of mobile phones are using a discrete solution. Ramping too fast will result in a spread of spectrum and a to slow ramping hurts the time constraints. The output power P_{out} of most power amplifiers PA and therefore for the complete TX system is set by an external voltage V_{Crtl}, but the relation between V_{Crtl} and P_{out} is often very nonlinear and influenced by temperature, tolerances, supply voltage, frequency and PA input power. Therefore to achieve sufficient accuracy in most cases an additional power control loop is needed, although some designers tried to use no-feedback concepts [1], e.g. by controlling the PA supply voltage. Such a control loop basically consists of a RF detector and a loop amplifier getting its input signal from the baseband controller (figure 1). Most differences in power control loops can be found in the detector, but also the loop amplifier has interresting design aspects.

II. Detector Design

One item in the power control loop design is the dynamic range. For a GSM mobile phone the maximum antenna power is 33dBm and the minimum power level is 5dBm. But because we want to work in a precise feedback loop the detector dynamic must be significantly higher, e.g. $\geq$ (33-5+6)dB=34dB, which is pretty close to what a good diode detector can give. Another reason for the need of a larger dynamic range is that in a TDMA system the PA starts from power down mode in which the RF level is determined by noise and crosstalk. This level should be lower than about -48dBm for the GSM system and would result in a dynamic range of over 70dB. If we now apply a voltage to the PA control input the output power increases. But due to the finite detector dynamic the loop is not locked and at the point the detector responds we may get a large overshoot. Also working in the power range near or below the minimum detectable signal the operation is generally strongly influenced by temperature, tolerances, etc. and all these problems will result in a longer calibration time in production. This - and not only bill of material BOM - is also important for the economic efficiency.

In most control loop designs diode detectors are used (together with directional couplers). A RSSI circuit would give a larger dynamic range but is not easy to realize at TX frequency [2], so this option is currently preferred only for base station designs, where the required dynamic range is significantly larger. For diode detectors the dynamic range is limited by the sensitivity reduction in the quadratic region. For multi-stage RSSI circuits there is a noise limit. DC offsets (also created by the loop amplifier) will also reduce the dynamic range, but this error can be eliminated by calibration, so only its drift is important. Other important design aspects are the temperature and supply dependance of $V_{Detect}(P_{in})$ (not only for the zero point but also for the gain coefficient), the detector speed (which is often very high, e.g. t_r<50ns) and the frequency dependance of the output voltage (simple diodes show often more flat response than typical directional couplers). Another detector solution would be to measure the PA supply current which is done in some older mobile phones. In this case the main drawbacks are the reduction in efficiency for todays low-voltage designs, noise and offset problems due to high gain needed and problems to compensate the power for changes in TX frequency and supply voltage [3]. It seems to be that a RSSI would be the ideal solution but there are also problems with this option concerning loop dynamics.

III. Loop Dynamics

Two things are making the loop design not easy. One is that some PA´s are not very fast, i.e. there might be a significant delay between a step at the control input and the change in output power. This limits the speed of the control loop and can cause instabilities. It´s a pitty that most PA data sheets

ignore this point. On most data sheets only a full step response time shorter than 1µs is guaranteed. Compared to the PA the detector and the loop amplifier (ignoring the dominant pole which is always needed in feedback systems) are much faster in good control loop designs.

The second problem is that especially the PA and many detectors are very nonlinear. Building a power control with an ideal linear detector and a linear control loop amplifier an ideal PA would have a constant slope $d\sqrt{P_{out}}/dV_{Ctrl}$, but in reality it depends on V_{Ctrl} and is often small not only at low power levels but also near compression. This results in a bias dependend overall loop gain and makes frequency compensation of the feedback system rather difficult (especially at mid-gain) and if the loop is stable the circuit might be too slow for some power levels. Many PA´s show a negativ slope in deep compression, so some safety margin is needed to prevent fold-over. The best situation would be that the non-linear dectector behavior matches the non-linear PA characteristic. In this respect a log-limiting amplifier RSSI with its linear-in-dB behavior is not optimum, because at high power levels this would result in a low loop gain and therefore slow ramping. Also the single diode detector is not optimum because at the low power end of its transfer characteristic sensitivity is reduced due to the quadratic behavior, although at high and medium power levels the diode detector works well (linear rectifier with constant slope). A very good solution would be to combine the high low-end RSSI sensitivity with the high high-end diode sensitivity. This can be realized using an additional gain-shaping block e.g. at the detector output. Of course this block should not introduce more offset (and noise). In this respect also the RSSI circuit is worse compared to the simple diode detector, so some accuracy of a RSSI circuit is lost although it´s overall behavior is superior at low levels.

IV. Additional Features

In FCC tests not everything is checked and although the device may pass the official examination there might be problems in real-world application. One example of such a case is the behavior on antenna mismatch. Here the system designers don´t want the PA to sink too much supply current, because this may also influence or even shut down the digital or other parts. Therefore some kind of mismatch protection is often needed (e.g. depending on the robustness of the PA design). This can be done either sensing the PA current or by detecting not only the incident wave but also the reflected. Both solutions might be equivalent, maybe the second one has the advantage that if the controller e.g. responds to the sum of both terms then simply the output power is reduced and no second feedback loop is introduced. Also the high-current shunt resistor for the current protection is not easy to implement (accuracy, efficiency reduction). In failiure mode the control loop amplifier output voltage may reach extreme values and may destroys the PA or latch up the loop due to roll-over ($dV_{Ctrl}/dP_{out}<0$). Therefore it´s good to limit the loop amplifier output voltage, e.g. to negative values for MESFET PA´s.

One reason why discrete control loops are so succesful even today (at least for single-band solutions) is their flexibility. For instance the coupling coefficient of the directional coupler should match the maximum input power of the RF detector. Another example might be a low-pass filter often needed after the DAC output to suppress noise and glitches. This is needed for some DAC´s but not for others. So a good IC design must give a good compromize between the number of external components and flexibility, e.g. when adapting different PA´s or baseband controllers. But of course also an IC solution has its advantages. In this case it is not only size, fast time-to-market and costs but also higher precision and higher speed resulting in lower calibration time.

V. Realization and Results

The chips are fabricated in a 26GHz bipolar technology also used for many standard RF IC´s (figure 2+3). The need for a RF detector and the availability of verticale pnp transistors (f_T=4GHz) and high density capacitors (2fF/µm²) are the main reasons for this choice. Different versions have been realized: V1 with internal detectors and one loop amplifier for a single-chain dual-band PA with switched-matching, V2 with external detector diodes also for a switched-matching PA and V3 with internal detectors and two loop amplifiers for a two-chain dual-band PA. All loop amplifiers are designed to directly drive a MESFET PA with a output voltage between -0.6V to -3V. But now also a single-supply version for modern HBT/MOS PA´s is designed for VQFN-20 package. V1 and V2 are housed in a TSSOP10 package and V2 in a TSSOP20, both with 0.5mm pitch. For V3 we use two independ op-amps and detectors.

For the RF detectors emitter followers are used (figure 4). This kind of circuit is similar to a diode detector but creates less harmonic distortions due to higher input impedance. Due to large RF input voltages (max. +13.5dBm in system operation) a high voltage npn transistor is needed (V_{EBO}>2V) and for good sensitivity the base resistance is minimized (double base contacts). After the detector a quasi logarithmic gain shaper using a base-emitter diode follows. To

compensate drifts both the RF signal and the control signal are going through the same signal chain. For the reflected power the detector sensitivity is reduced, so that small mismatches at the antenna will not influence the control loop. Both inputs have 50Ω impedance, with very low VSWR (typically smaller than 1:1.05 including package parasitics!). The detector output voltage at lowest power level is only a few mV, so a high precision control loop amplifer is needed.

The control loop amplifier design is quite straight forward because - as in the old days - a negative supply V_{EE} is available (figure 5). Basically it is a two stage op amp design and both stages use emitter followers to achieve sufficient open-loop gain (80dB) and low input bias currents (I_B<10nA). The all-npn output stage is choosen because of high bandwidth (op amp GBWP 40MHz, slewrate 4V/µs) and the voltage range matches the MESFET PA requirements (low voltage drop at the negative rail). Frequency compensation is done by a single Miller capacitor. The total offset drift of both the detector and the op amp is typically lower than 1.5mV for a 100°C temperature range and an supply voltage change of 1V. This is much better than for a typical discrete design.

The design for a single supply solution (e.g. for MOSFET or HBT PA´s) is more difficult because of the pnp CE output stage needed and the restrictions on common mode input range due to low supply voltage V_{CC}.

Due to the low detector output voltage at the lower end of the dynamic range, many effects will influence the accuracy. The main influences are the detector offset drift (due to physically small structures for good RF performance), the frequency dependance of the the directional couplers and RF filters, but also the DAC resolution (10 bits are sufficient) and its drift might be important. The calculation also shows that although the system tolerances are tighter at the high power GSM levels they are easier to achieve.

Not only sufficient static accuracy is needed, the low loop gain and speed at small power levels is even more critical. At the begin of the TDMA burst the PA must be in cut-off, so the control voltage $V_{Ctrl}(t=0)=V_{Home}$ must be more negative than the gate turn-on voltage V_{TO} (due to self-biasing this depends also on PA input power). Due to PA tolerances some voltage margin is needed (e.g. 0.4V depending on MESFET process), but this will result in a variation in delay time (e.g. some µs) of the power-time characteristic. To fullfill the power-time template you need either a very fast loop, low component tolerances or more calibration time. Also important is that V_{TO} depends also on temperature and PA supply voltage V_{Bat} (many modern PA´s are operating directly from a LiO battery for high efficiency and low cost). So in our design we implement a compensation of V_{Home} for changes in V_{Bat} and temperature to decrease delay tolerances. The coefficients are optimized for a typical GaAs MESFET PA and are programmable via metal mask. Maybe the best way to provide a home position might be a dummy stage on the PA die. The only remaining errors in this solution are matching errors and threshold shift due to self biasing due to RF input power. This solution can be implemented in our chip via metal masks.

VI. Conclusions

A TDMA power loop controller and its theory is presented. Due to the minimum component count this solution can economically replace older discrete solutions. Special care has been taken not only to minimize BOM but also calibration time during manufaction. Also the gain shaping block offers some possiblities for improved operation. A next step would be circuit optimization for our single-supply PA controller and a control loop containing a S&H circuit for non-constant envellope systems like EDGE. For the near future it can be expected that the power control will move into single-chip BiCMOS transceivers.

References

[1] "Triple band dual mode power amplifier application board for GSM/DCS1800/DECT", Motorola, Microwave Engineering Europe February/March 1997, p.27-28

[2] Analog Devices, AD8314 data sheet (2GHz RSSI)

[3] Maxim, MAX 4473 data sheet (PA Controller)

Figure 1:
Basic structure of the discussed power loop (NVG and supply switch is only needed for GaAs-FET PA´s)

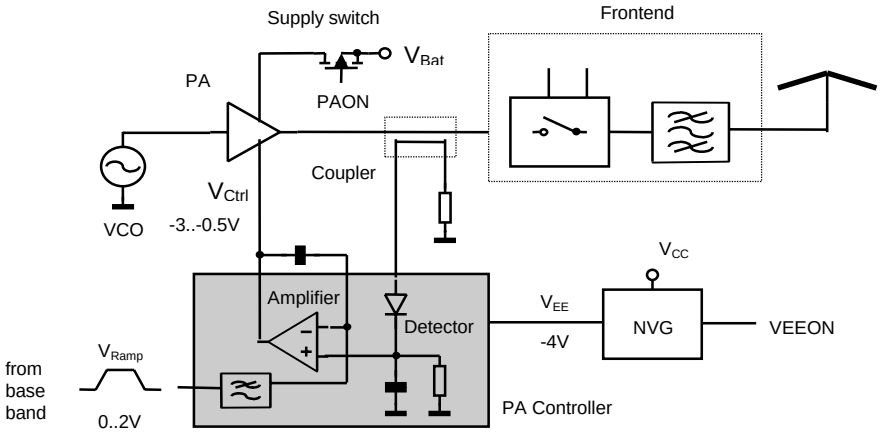


Figure 2:
Block diagram of the circuit V1 (gain shaper within detector blocks)

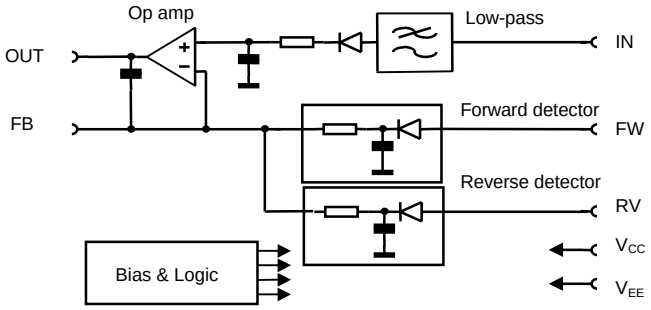
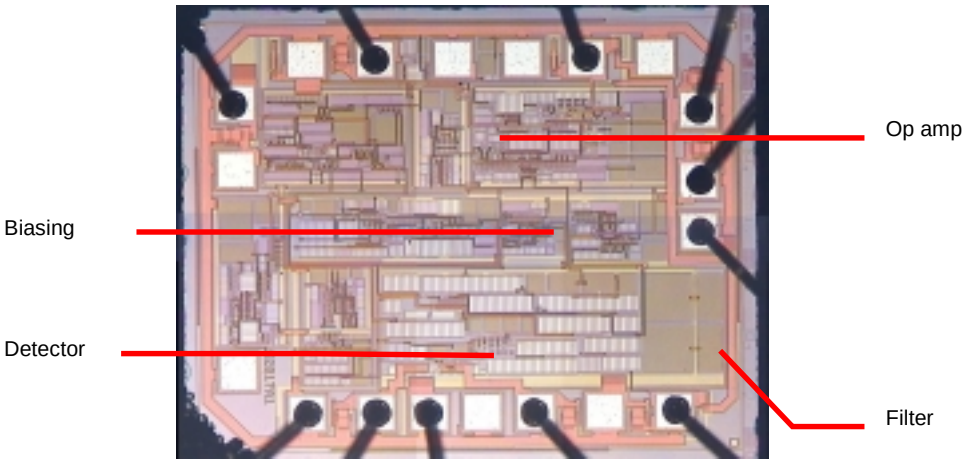


Figure 3:
Die photo V1 (area 1,3mm²)



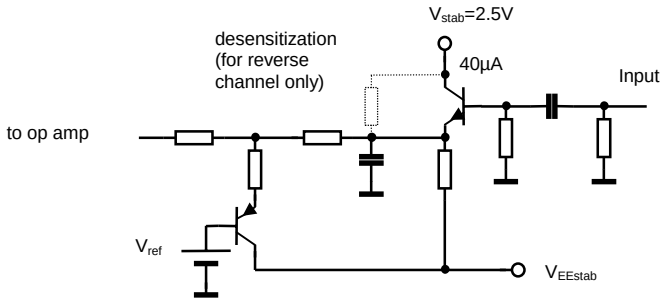


Figure 4: RF detector and gain shaping block

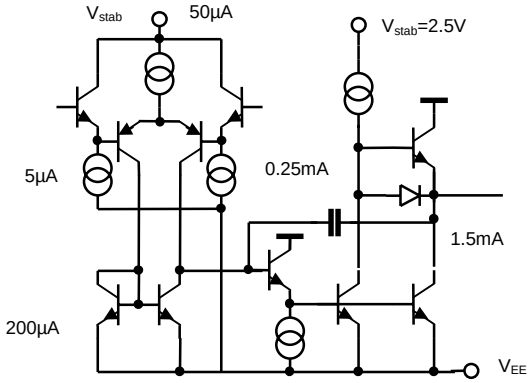


Figure 5: Basic op amp circuit