Modeling for Si-Bipolar Power Amplifiers

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Abstract

Designing RF PA´s you will propably find a too large difference between simulation and measurements. Therefore accurate modeling of all used parts is needed to make simulation becoming an accurate design tool. The most important parasitic influences are identified and their modeling is shown.

1. INTRODUCTION

The market of RF power amplifiers for mobile communication is presently dominated by GaAs MESFET technology. At the low frequency end (e.g. GSM f_o=900MHz) or at low power levels (e.g. DECT P_{Ant}=250mW) Si BJT or MOSFET technology is becoming more important, due to their lower die costs and the possibility for a higher level of integration. For GaAs there are also further drawbacks e.g. the need for a supply switch and the negative gate voltage. Because there is still a drawback in Silicon compared to GaAs in respect to high frequency performance, especially at high powers (e.g. f_T, f_{max}, breakdown voltages, no chip vias in Si, large substrat losses, no thick Au metalization, etc.) you must get maximum performance from your Si technology.

This performance is not only limited to the intrinsic devices, e.g. described by $f_T(I_C)$ etc., but also by parasitic elements, e.g. in the substrate, die interconnections, package, thermal performance and external components (especially in the matching networks). An accurate modeling for the active desvices and all the parasitics is needed (figure 1).

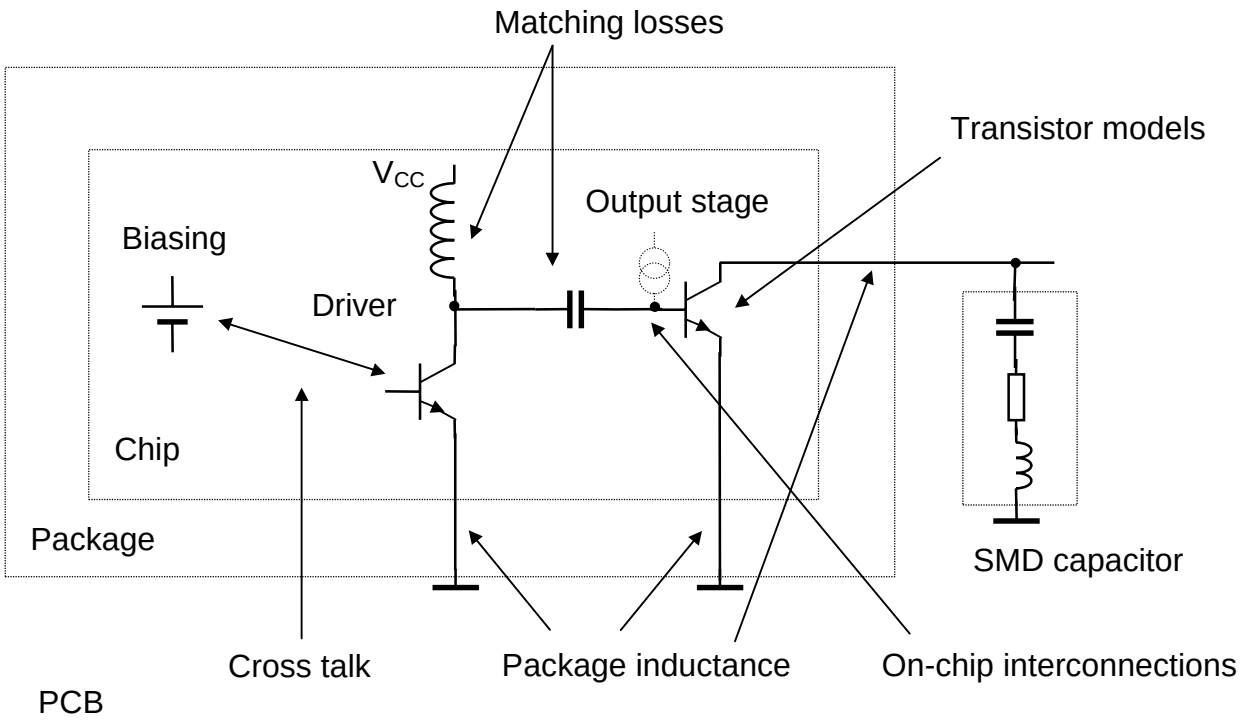


Figure 1 : Some of the main modeling problems in RF PAs

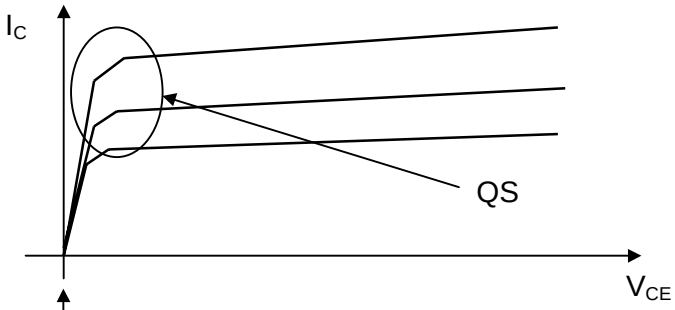
2. MODELING THE BJT

In most standard circuit simulators like SPICE, SPECTRE, SABER, etc. only the Gummel-Poon model is included, maybe with some extensions. In the case of RF PA´s first you need good parameters for this basic model. Often even the GP parameters are not fully understand by the users and some of them are only guessed or even at their default values. In real world PA´s also the reverse parameters (e.g. the transit time TR) and the series resistances becomes very important. There are also some effects not included in the GP model at all (figure 2). To model the quasi saturation region or the accurate dependance of f_T vs bias conditions and temparature you need extended models. Using high f_T-technologies you may get problems with breakdown voltages [1]. For a typical 20GHz-f_T-transistor the V_{CEO} is only about 4.5V. The V_{CER} or V_{CBO} is much higher (about 15..20V) but in reality the maximum usable collector-emitter voltage is between this limits. As a rule of thumb the supply voltage V_{CC} should not ecxeed V_{CEO}, the RF swing gives then higher collector voltages up to 2 .. 3 times V_{CC} (due to inductice load and the influence of the harmonics) [2]. This margin is needed to get safe operation even in the presence of large VSWR values and production tolerances. Some further margin may be achieved by a low impedance drive of the RF transistors because V_{CER} depends strongly on I_C and the source resistance R itself. Transistor characterization is most important for the output devices. If you cannot extract data directly from the large output structures you need to extrapolate from smaller structures. This should not be done by simply using the area factor because e.g. the ratio between edge and area capacitances changes with the transistor size. If the amplifier works in saturation mode (in most systems like AMPS, GSM, DECT) accurate transistor modeling is important not so much for the simulation of the output power and efficiency but more important to design the driver stage and the interstage matching.

Figure 2 : a) Some draw backs in standard BJT models

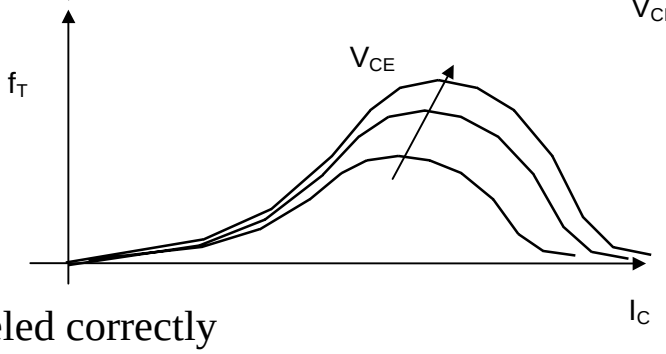
Quasi saturation

New parameters needed
Known models are quite unaccurate
Dynamic parameters also changed



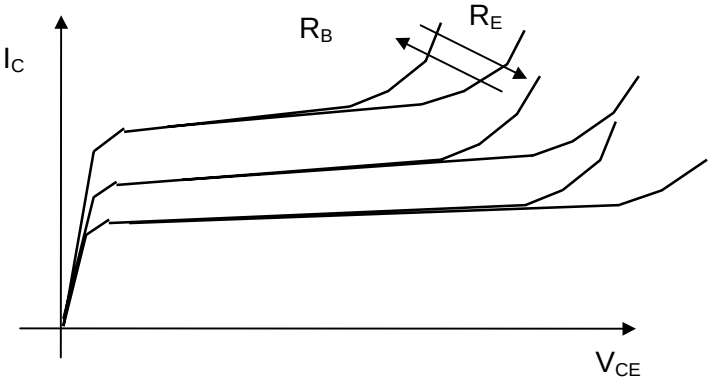
f_T-curve

SPICE model with TF, XTF, ITF,
VTF is not sufficient
Temperature dependance and low voltages/high currents are not modeled correctly



Breakdown

You have to look at V_{CEO}, V_{CBO} and most important V_{CER} which depends on current and resistors



b) Influence of transistor performance on an 1.9GHz-PA

Technology	f_{Tmax}	V_{CEO}	V_{CER}	V_{CCmax}	P_{out}	PAE
#1	≈26GHz	4.0V	16.3V	4.1V	28dBm	39%
#2	≈16GHz	6.9V	18.6V	5.4V	27dBm	36%
#3	≈19GHz	4.1V	20.9V	6.1V	27dBm	35%
#4	≈10GHz	8.7V	21.0V	>7V	25dBm	28%

3. ON-CHIP INDUCTORS AND DIE INTERCONNECTIONS

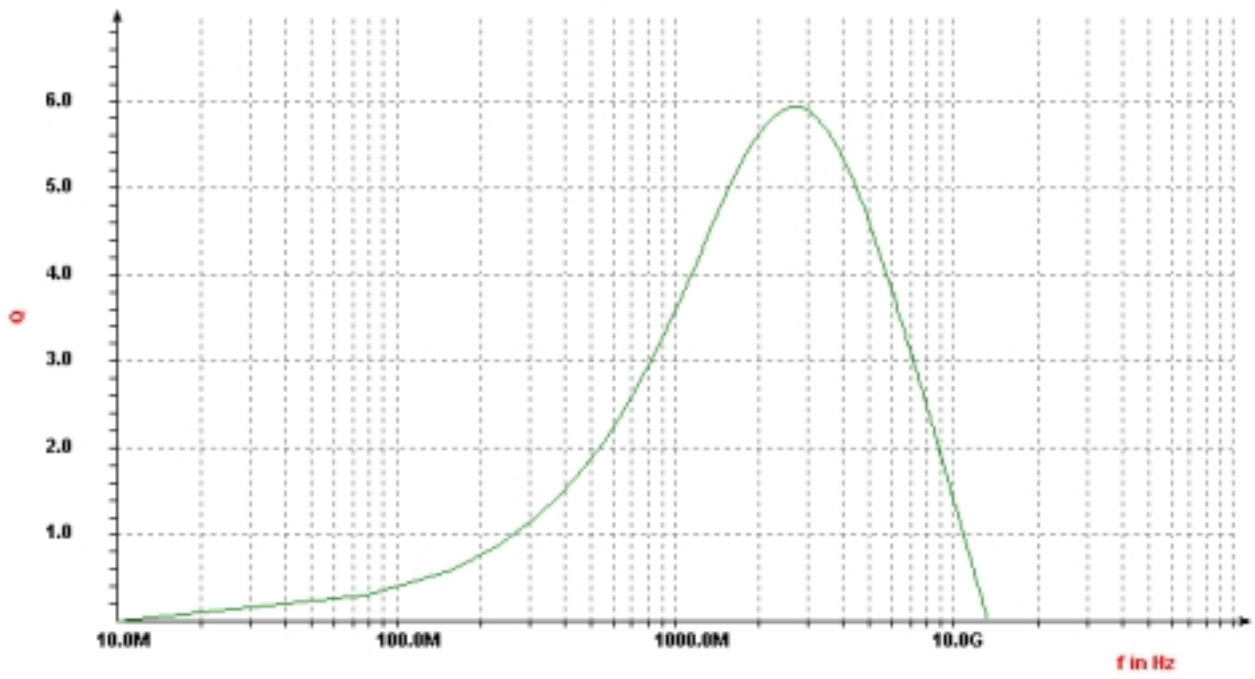
In modern RF technologies with an f_T of 20GHz or more RF amps often looks like AF amplifiers. But at high power levels (e.g. >10mW depending on frequency) you get much better performance in respect to noise, stability, spurious rejection and efficiency using on-chip inductors [3,4] (figure 3) instead of RC coupling. In a standard Si technology with 3 Al layers and a substrate resistance of 10Ωcm you get coils with maximum Q factors of about 5 to 8 (typically at 1 to 3GHz) with inductances of 1 to 8nH and areas of about 100x100µm² to 400x400µm². 2½ or 3-D field simulators, test chips or special programs are useful to understand on-chip coils. A π-circuit model with L_s, R_s, C_{ox} and R_{sub} is almost sufficient for circuit analysis up to 2GHz.

Figure 3 : a) Typical configurations of on-chip inductors

Variations : Tapped coils, center tapped coils, coupled coils

Hints : Use large coils for low frequencies to minimize series resistance and use smaller ones at high frequencies to minimize substrate loss. Do not use the center of the coil, because inner turns have small inductance but some series resistance. Use upper metal layers, not metal 1.

Figure 3 : b) Typical graph Q vs f (L is 4nH) :

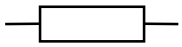


In some CAD systems you may get an extraction of the parasitics in the interconnections [5]. But many of these tools are written for digital or low power circuits, so they are looking only at the series resistances and the parasitic capacitances to the substrate but magnetical coupling is not included (figure 4 to 7). In the case of RF power amplifiers the impedances becoming quite low (few Ohms at the input of the power transistors), therefore the series inductances is in many cases much more important than the shunt capacitances. In Si technology with a substrate height of about 300µm you get about 0.5 to 1.4nH/mm inductance per length (depending on width and distance to ground planes). Using large structures like on-chip inductors, MOS capacitors with some pF or output power transistors the length of interconnections is very different from zero, e.g. a line of 300µm (e.g. from the driver output to the base input of the power stage) may gives an impedance of about j3Ω at 2GHz (figure 8). This is often much more than the ohmic part and in the range of the input impedance at the base of a power transistor.

Accurate modeling of the on-chip coils and the interconnections is very important for the design of the interstage matching and has a great influence on the frequency response of the PA.

Figure 4 : Parasitics in on-chip interconnections

$R = R' \cdot l = R_{sheet} \cdot l/w$

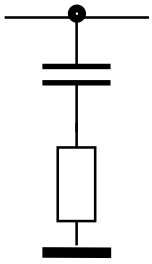


=> Voltage drop, damping, noise

$L = L' \cdot l$

=> Phase shift and impedance transformation

$C = C' \cdot l = \varepsilon_o \cdot \varepsilon_r \cdot l \cdot w/d_{ox}$ + edge capacitances



=> Damping, cross talk and substrate coupling

Figure 5 : Ohmic series losses

$R = R' \cdot l = R_{sheet} \cdot l/w$ 

Example : l=0.5mm, w=10µm			50Ω-System	5Ω-System
Al1 50mΩ	=> 2.5Ω	=>	-0.215dB	-1.94dB
Al2/3 30mΩ	=> 1.5Ω	=>	-0.13dB	-1.21dB

(5Ω is approximately the typical input impedance at the base of an output power transistor)

Skin effect : δ = 1.8µm at 1.9GHz => only small influence!

=> Interconnetion is critical

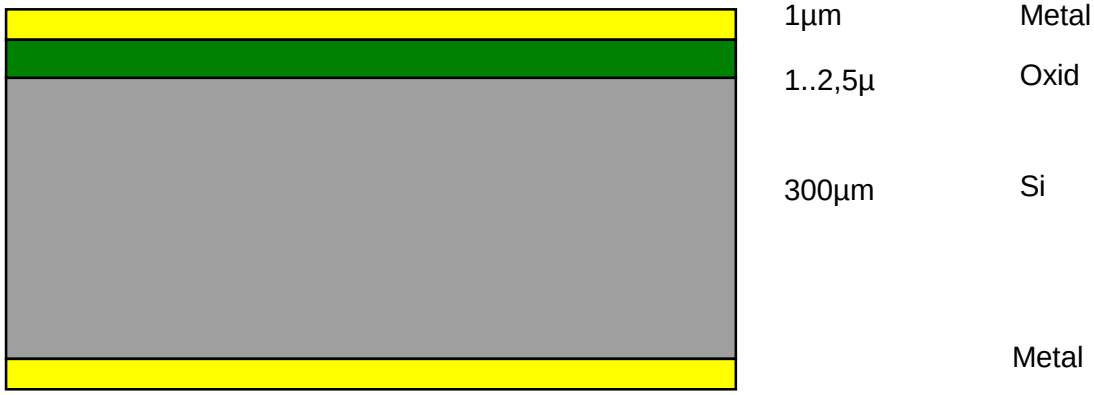
=> Series resistances of integrated MOS capacitors are critical

Figure 6 : Transmission lines

$Z_L^2 = R' + j\omega L' / (G' + j\omega C') \approx L'/C'$ (for low loss lines, but not on Si!)

$v = c_o/\sqrt{\varepsilon_{r(eff)}} \approx 1/\sqrt{L'C'}$

$L = L' \cdot l$



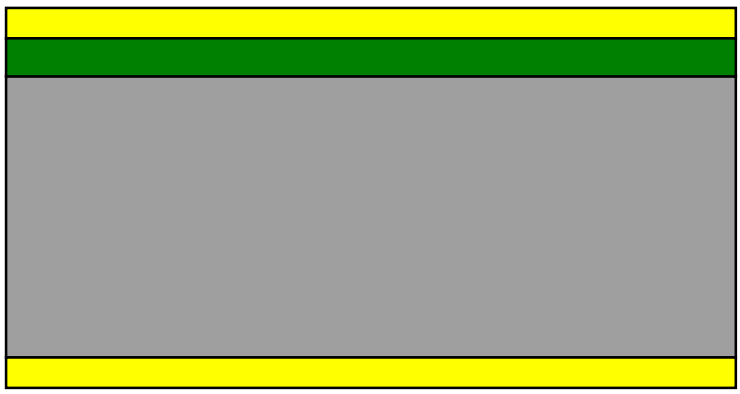
H-field comes deep into the substrate

=> effective distance ≈ d_{sub} (typical 300µm) => L´ is relative large!

w	L´ (calculated as microstrip line)
2µm	1.4nH/mm
5µm	1.23nH/mm
10µm	1.09nH/mm (about 7Ω for 500µm at 2GHz)
25µm	0.9nH/mm

L´s is smaller for odd mode , but not so much

$C = C' \cdot l = \varepsilon_o \cdot \varepsilon_r \cdot l \cdot w / d_{ox}$ + edge capacitances



E-field stops at the Si surface (because $\omega\varepsilon E << \sigma E$)

=> effective distance ≈ d_{ox} (typical 2µm) => C´ high + series resistance

w	C´ (Alu2, calculated as microstrip line)
2µm	≈65fF/mm
5µm	≈110fF/mm
10µm	≈190fF/mm (about 800Ω for 500µm)
25µm	≈440fF/mm

In low impedance circuits (as PAs) the series losses are much more critical than the capacitances to substrate.

=> Layout should optimized not for minimum C_{sub}, but minimum L_s+R_s

Figure 7 : Transmission line parameters

w	Z_L (at low frequencies)		
2µm	≈146Ω	=>	Z_L has typical values, but it is now
25µm	≈50Ω		complex and frequency dependant

w	v_{ph}	ε_{reff} (at low frequencies)		
25µm	≈50Mm/s	35	=>	ε_{reff} is very high
2µm	≈100Mm/s	8	=>	much phase shift & transformation

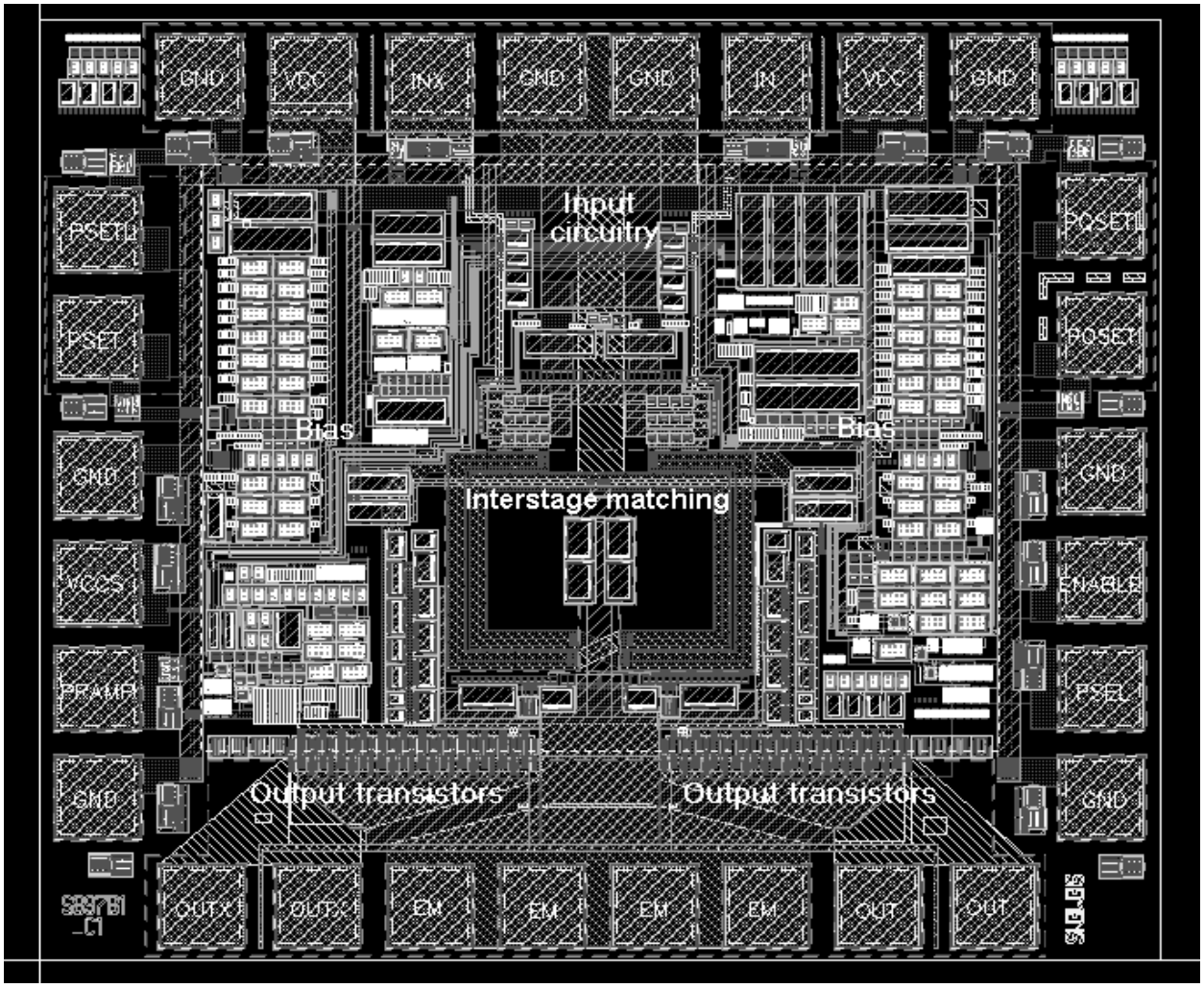
=> **„Slow-Wave-Mode“**

What is more important R_s or L_s?

w	$\omega L/R = Q_s$ at 2GHz
25µm	9.4!!
2µm	2

=> **Series inductance is more critical (due to impedance, not noise) than the ohmic part**

Figure 8 : Layout of a balanced 1.9GHz-DECT-PA



=> There are many parasitics

4. SUBSTRATE AND PACKAGE MODELING

The package has a strong influence of the RF performance. There is much literature available and accurate modeling is one important key for a good RF PA design. This sounds simple but practice has shown that the package influence is in many cases more critical then the simulation shows. Therefore there is much to do and if you get a complete model you have to asks if it is this really correct. What are the limitations, e.g. in frequencies? Is the model based on physics? Is there a comparision between simulation and modeling? The only way seems to be to make a model which bases both on 3D-field simulations and measurements. For PA´s this model has to include also the losses due to ohmic resistances, skin effect and dielectric. The package influence is of cause most important for the output and the ground pins. Good grounding conditions are needed for high RF gain, good stability and isolation. Error voltages on ground plane or in the substrate [6] often have a negative influence on the bias circuit. Using not to low bias currents and guard rings for the isolation between RF and bias circuits is important to minimize these effects. The subtrate losses also cause a drop in RF gain which has to be modeled. Our simulations also shows, that using a single subtrate node (like in small signal IC´s) is far from reality and not sufficient.

5. MATCHING NETWORKS AND EXTERNAL COMPONENTS

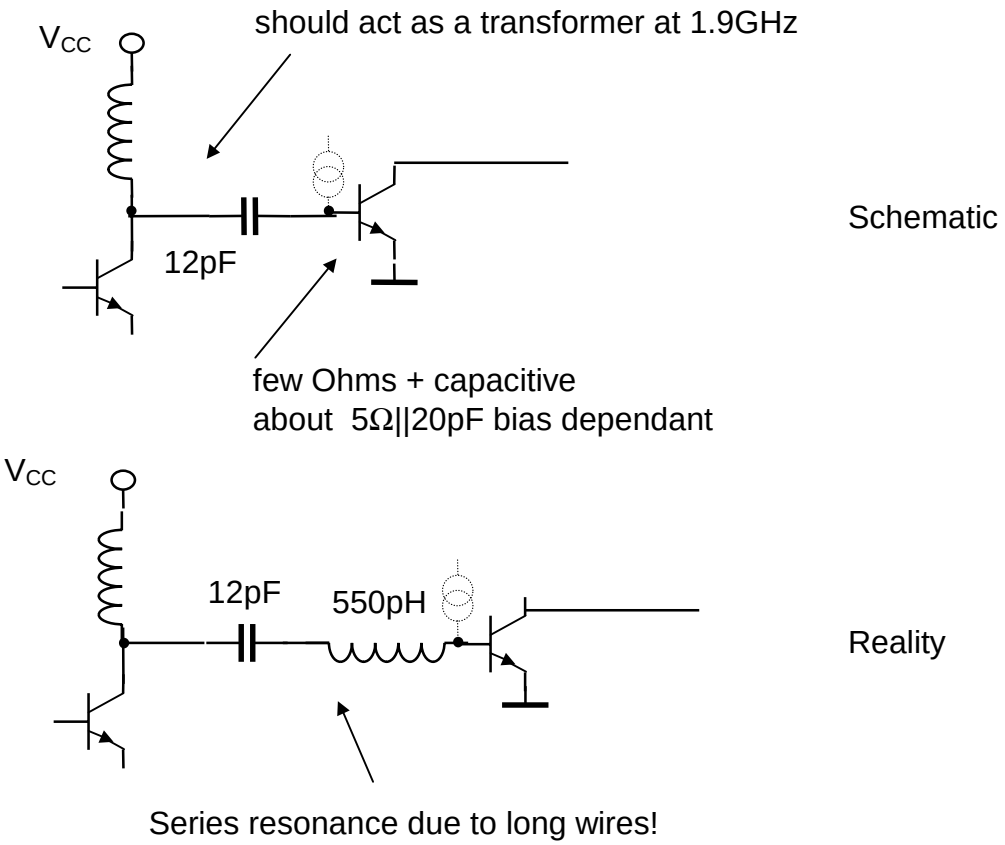
For high output power levels you need an external matching network because you get too much losses with on-chip elements which reduces the efficiency. It also appears that it is not possible to design the linear impedance transformation networks only by linear simulation due to influence of the harmonics (especially for high power amplifiers). Therefore it is better to use a time domain/harmonic balance simulator (e.g. APLAC) to optimize the matching elements in conjunction with the nonlinear output stage. As a starting point it is of cause suitable to use e.g. Smith diagram technics or a linear circuit simulator with an optimizer (like Touchstone, SuperCompact or APLAC).

Designing a balanced amplifier you get a better performance in respect to substrate coupling, ground noise, harmonics etc. But an output balun is not easy to design and has maybe higher losses than a simple matching network. Also the influence of the ground inductance is only effectively reduced in near class A operation. Decoupling is also important for PA´s. The supply impedance should be low not only at the frequency of operation f_o but also from DC to about $3 \cdot f_o$.

Figure 9 : Parasitics in a typical RF PA

Part	**Influence**	**Comments**
Transistor models	May have a large influence, especially on interstage matching !	GP may be sufficient, but not in all cases. High current/low voltage region is critical!
Capacitances to substrate	Often a low influence (not for transistor or MOS-C capacitances)	This is different to low power/high impedance designs.
Series resistors	Medium influence. Look also at the MOS capacitances	Reduces gain
Series inductances	Large influence ! Not only as feedback in BJT emitters stages	Changes frequency response
On-chip coils	Medium influence. A Q of 5..7 is realistic. You have to include the lines to the coil	Modeling is not too difficult, but Q is limited for typical Si technologies
Package model	Strong influence due to series inductances	Difficult to model
Substrate model	Medium influence on bias and RF performance	Difficult to model, important for mixed mode designs

Figure 10 : Influence of interconnection parasitics for interstage matching



=> Collector of the driver directly connected to the low impedance base

=> Only small voltage swing at the collector

=> Driver current must be very high, due to mismatch!

=> Resonance frequency is too low, low efficiency

=> Even the circuit topology may be changed due to parasitic elements not only the parameter values

6. CONCLUSIONS

Accurate simulations are possible for RF power amplifiers, but only if all parasitics are modeled correctly (figure 9). In practice this is often not the case and also hard to reach at all. If you want to build not only a single PA then the additional design effort should be accepted, because parasitic elements not only influence the performance but may also modify your topology (figure 10). If you want to create a new design you get a much better starting point because much of the needed knowledge is in your models.

Literature :

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